IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Yamazaki, et al.	Art Unit	: 2813
Serial No.	: 09/898,986	Examiner	: Laura Schillinger
Filed	: July 3, 2001		
Title	: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Supplemental to the Information Disclosure Statement filed with this application on July 3, 2001, Applicant submits the attached Form PTO-1449, listing references that are of record in parent cases having Applicant Nos. 09/272,701 (filed March 18, 1999) and 08/890,591 (filed July 8, 1997).

Although the listed references are of record in this Application, as well as in the above-mentioned parent applications, this IDS is being filed to provide, for the Examiner's convenience in initialing, a clean listing of the references on the attached Form PTO-1449.

The references cited on the attached Form PTO-1449 were submitted to and/or cited by the Office in the prior applications and, therefore under Rule 97(d), are not provided in this application.

Inasmuch as the listed references are of record in the above-mentioned parent cases (and because the listed references were included with the July 3 IDS), no fee is believed to be due. In the event that any fee is due, please apply any charges or credit any overpayment to Deposit Account No. 06-1050.

Respectfully submitted,

Date: July 11, 2003

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Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 07977-163003	Application No. 09/898,986
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Yamazaki, et al.	
		Filing Date July 3, 2001	Group Art Unit 2813

U.S. Patent Documents

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	5,898,204	4/1999	Watanabe			
	AB	5,998,854	12/1999	Morishita et al.			
	AC	6,180,957	1/2001	Miyasaka et al.			
	AD	5,550,397	08/27/96	Lifshitz et al.			
	AE	5,552,624	09/03/96	Shotnicki et al.			
	AF	5,616,935	04/01/97	Koyama et al.			
	AG	5,659,192	08/19/97	Sarma et al.			
	AH	5,726,459	03/10/98	Hsu et al.			
	AI						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AJ	04-206971	07/28/92	JAPAN				
	AK	04-286339	10/12/92	JAPAN				
	AL	06-232059	08/19/94	JAPAN				
	AM	07-169974	07/04/95	JAPAN				
	AN	07-176753	07/14/95	JAPAN				
	AO	07/321339	12/08/95	JAPAN				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AP	Wang et al., Enhanced Performance of Accumulation Mode 0.5 μm CMOS/SOI Operated at 300 K and 85 K, IEEE, IEDM 91, pp. 679-682.
	AQ	Fossum et al., "Anomalous Leadage Current in LPCVD Polysilicon MOSFET's", September 1995, IEEE Transactions on Electron Devices, Vol. ED-32, No. 9; pp. 1878-1884.
	AR	Qian et al., "Inversion/Accumulation-Mode Polysilicon Thin-Film Transistors: Characterization and Unified Molding", September 1988, IEEE Transactions on Electron Devices, Vol. 35, pp. 1501-1509.
	AS	Malhi et al., "p-Channel MOSFET's in LPCVD Polysilicon", October 1983, IEEE Electron Device Letters, Vol. EDL-4, No. 10, pp. 369-371.

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	